

REMARKS

Claims 1-23 are pending in this application. Claims 1, 14, 16, 18 and 21 are the independent claims. No claims are amended in response to the outstanding rejections.

Allowable Subject Matter

Claims 10-12 are indicated as being allowable if rewritten in independent form to include the features of their base claim and any intervening claims. Claims 10-12, as well as the remaining pending claims are in condition for allowance for the reasons discussed above.

Rejections under 35 U.S.C. §103

Claims 1-9, 13-17 and 21-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,506,874 to Izzard et al. (Izzard) in view of US Patent Application Publication 2004/0096013 to Laturell, et al. (Laturell). Applicants respectfully traverse this rejection for the reasons detailed below.

It is admitted in the Office Action that Izzard fails to disclose “four latches controllable to latch, at different times according to quadrature clock signals, respectively, data received by the quarter-rate phase detector so as to form latched signals.”

In an effort to overcome the admitted deficiency, Laturell is combined with Izzard and it is alleged that one of ordinary skill in the art would have modified the device of Izzard according to the teachings of Laturell.

Laturell relates to clock recovery and data recovery systems. In Laturell, a parallel transmit (XMT) data vector 102 is fed to a transmitter 104 that receives the parallel data along with the differential transmission clock from transmitter-local voltage-controlled oscillator (VCO) and/or phase-locked loop (PLL) 106. The transmitter loads the parallel data into a shift

register and uses I and Q clocks to generate a transmit clock, which is used to serially "clock-out" the contents of the shift register. The resulting serial data out 108 is output from transmitter 104 and transmitted across transmission medium 110 to a receiver 114. At the receiver 114, the serial data in 112 is received, sampled with a local clock that is a function of I and Q clocks from receiver-local VCO/PLL 116, and deserialized into parallel receive (RCV) data vector 118, which is output along with RCV clock (PRC) 120.

The receiver includes a front-end 202, a data recovery circuit 204, a clock recovery circuit 206, and a local clock generator 208. The local clock generator circuit 208 uses MIXO to generate quarter-rate local sampling clocks CLK2I, CLK2IB, CLK2Q, and CLK2QB, and the data recovery circuit 204 is used to divide down and further shift out the local sampling clocks to provide the parallel data receive clock PRC 120.

The front-end 202 also includes four integration circuits 302, 304, 306, and 308 and two edge samplers 310 and 312, each of which receives SDIN 112 and one of the four clock signals generated by local clock generator 208. The front-end 202 has six latches 314, 316, 318, 320, 322, and 324, each of which receives a differential signal pair S_i from a corresponding integrator or edge sampler, $i=1$ to 6. Each latch corresponding to an integrator outputs a different bit of 4-bit output data vector OD, and each latch corresponding to an edge sampler outputs a different bit of 2-bit output timing vector OT.

Assuming *arguendo* that one of skill in the art would seek to modify the device of Izzard according to the teachings of Laturell, modifying the phase detector of Izzard according to the teachings of Laturell would likely render Izzard unusable. For example, as disclosed in Izzard, and repeatedly argued during prosecution, the quadrature clock signals of Izzard (I, Q) are not used to control latching of the latches, but rather are used as data inputs. It is the clock signal D in Izzard that controls latching.

Therefore, modifying Izzard such that the quadrature clock signals (I, Q) control latching would completely alter the circuit design of Izzard. For example, the clock signal D would no longer be useful for its intended purpose (i.e., controlling latching) and the data signals (I, Q) would no longer be useful for their intended purpose (i.e., data inputs). Thus, simply modifying Izzard to include “four latches controllable to latch, at different times according to quadrature clock signals” would not render the rejected claims obvious, because Izzard would no longer function for its intended purpose (see MPEP §2143.01(V),(VI), 2143.02).

Regarding claim 7, it is alleged that Izzard discloses a multiplexing unit (identified as multiplexer 24 in rejecting claim 1) that includes a first and second multiplexers 28, 32 (Fig. 9). However, the multiplexers 24, 28, 32 are individual multiplexers, as shown in Fig. 9. The multiplexer 24 is not a “multiplexing unit that includes” first and second multiplexers 28, 32.

Regarding claim 8, it is alleged that Izzard discloses that the latched signals are pairs of latched signals, and each pair has a first set and a second set, “the second set representing the latched signals subsequently closest in time to the first set, respectively.” Specifically, it is alleged that the feature is disclosed at column 3, lines 14-19, of Izzard. However, there is nothing in the cited section of Izzard that indicates that the second signal (MI’’) is closest in time to the first signal MI’. Rather, the cited section merely recites that the output of the XOR gate 22 is coupled to the second data input multiplexer 24 and that the input signal D is coupled to the select input of multiplexer 24 that provides a method of choosing between the two command signals MI’ and MI’’ depending on which is selected.

Regarding claim 9, it is alleged that XOR gates 20, 22, 26 and 30 of Izzard each receive one of the pairs of latched signals. However, as shown in Fig. 9, the alleged pair of signals (MI’ and MI’’) is received at each of the XOR gates.

Regarding claim 10, it is alleged that Izzard discloses a second set of latches (14a, 14b, 18a, 18b) that receives the outputs of the first set of latches (12a, 12b, 16a, 16b). However, as clearly shown in Fig. 9, both sets of latches receive the same signals and the outputs of each are output from the MUX 24. There is nothing to suggest that the output of the alleged first set of latches is received by the alleged second set of latches.

For at least the above reasons, the Applicants respectfully request that the rejection be withdrawn.

Claims 18 and 19 stand rejected under 35 U.S.C. §103(a) as being unpatentable Izzard in view of U.S. Patent No. 6,847,789 to Savoj, et al (Savoj). Applicants respectfully traverse this rejection for the reasons detailed below.

It is alleged in the Office Action that Izzard discloses “the phase detector being controllable by the output of the VCO” (voltage controlled oscillator). However, Fig. 11 of Izzard shows a phase detector 10 and voltage controlled oscillator (VCO) 38. Izzard states that the output of VCO 38 in FIG. 11 is the quadrature clocking signal I [column 6, lines 23-24]. As described above, the quadrature clocking signal I does not control the phase detector 10, but rather, I is used as a data input to one or several of the latches of the phase detector 10, as shown in FIG. 1 of Izzard. Thus, the phase detector 10 of Izzard is not controllable by the output of the VCO 38.

In contrast, independent claim 18 recites a clock and data recovery circuit including a phase detector, “the phase-detector being controllable by the output of the VCO”. Again, signal D controls the phase detector by controlling the latching of the latches in the arrangement according to Izzard, and signal D is not the output of VCO 38. Furthermore, Savoj fails to cure

the deficiencies of Izzard, and thus, the combination of Izzard in view of Savoj fails to teach or suggest all the features of independent claim 18.

Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claim 20 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Izzard in view of Savoj and further in view of Laturell. Applicants respectfully traverse this rejection for the reasons detailed below.

Claim 20 is allowable for its dependency on independent claim 18, for the reasons discussed above. Further, as Laturell fails to overcome the deficiencies of Izzard and Savoj, the combination of references does not render the rejected claim obvious.

The Applicants, therefore, respectfully request that the rejection be withdrawn.

CONCLUSION

In view of the above remarks and amendments, the Applicants respectfully submit that each of the pending objections and rejections has been addressed and overcome, placing the present application in condition for allowance. A notice to that effect is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to contact the undersigned.

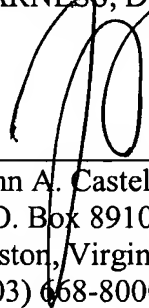
Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano, at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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